

FIG.1A
PRIOR ART

+	+	+	+	+	+	+	+
-	-	-	-	-	-	-	-
+	+	+	+	+	+	+	+
-	-	-	-	-	-	-	-
+	+	+	+	+	+	+	+
-	-	-	-	-	-	-	-
+	+	+	+	+	+	+	+
-	-	-	-	-	-	-	-

FIG.1B
PRIOR ART

-	-	-	-	-	-	-	-
+	+	+	+	+	+	+	+
-	-	-	-	-	-	-	-
+	+	+	+	+	+	+	+
-	-	-	-	-	-	-	-
+	+	+	+	+	+	+	+
-	-	-	-	-	-	-	-
+	+	+	+	+	+	+	+

09654943-090100

FIG.2A
PRIOR ART

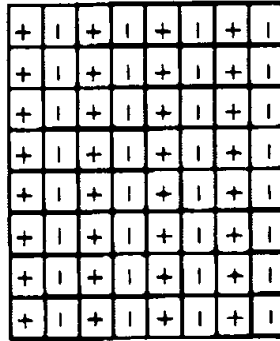
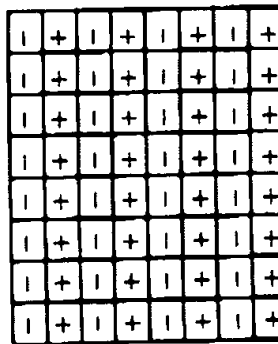


FIG.2B
PRIOR ART



09654943.050100

FIG. 3A
PRIOR ART

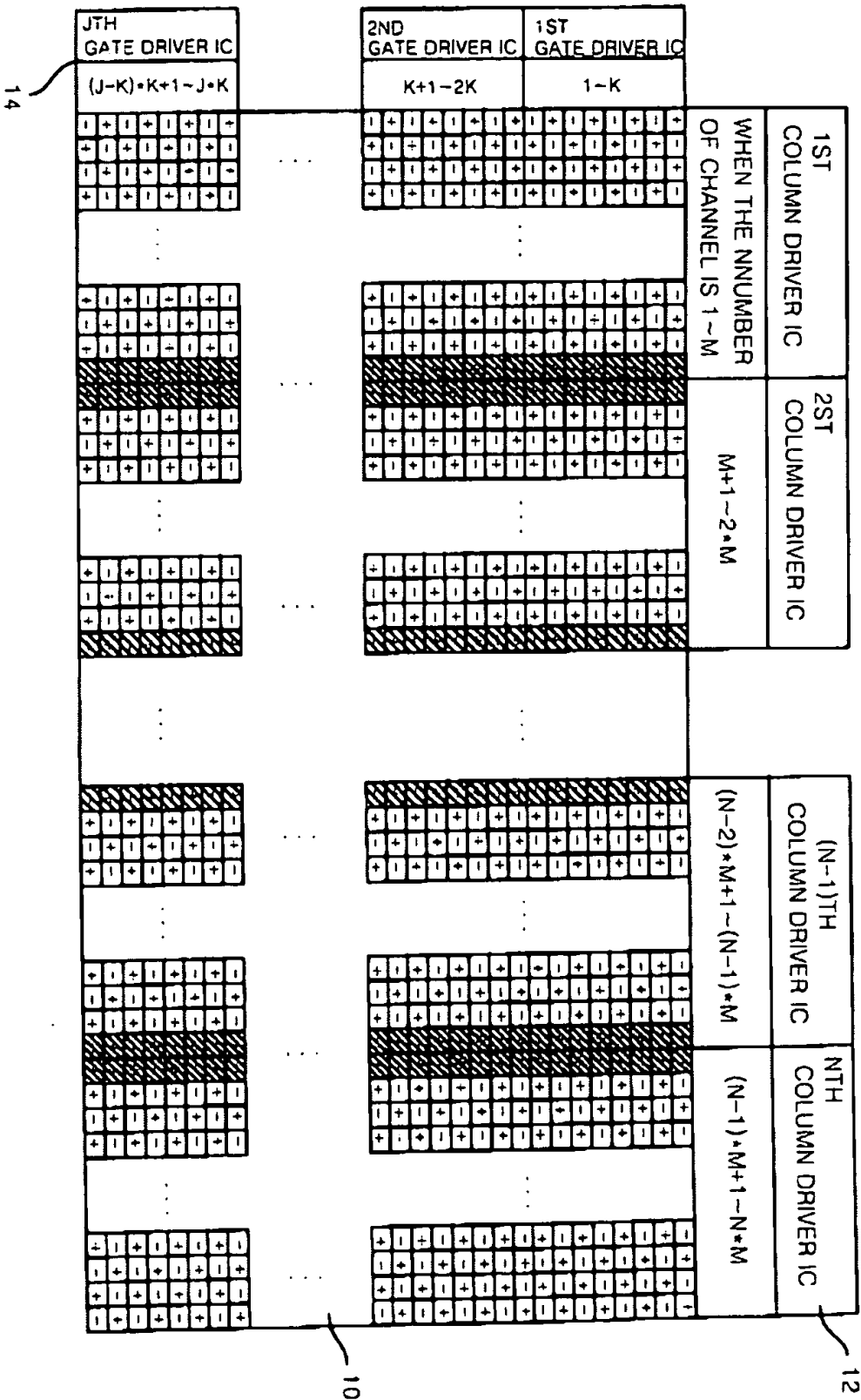
+	-	+	-	+	-	+	-
-	+	-	+	-	+	-	+
+	-	+	-	+	-	+	-
-	+	-	+	-	+	-	+
+	-	+	-	+	-	+	-
-	+	-	+	-	+	-	+
+	-	+	-	+	-	+	-
-	+	-	+	-	+	-	+

FIG. 3B
PRIOR ART

-	+	-	+	-	+	-	+
+	-	+	-	+	-	+	-
-	+	-	+	-	+	-	+
+	-	+	-	+	-	+	-
-	+	-	+	-	+	-	+
+	-	+	-	+	-	+	-
-	+	-	+	-	+	-	+
+	-	+	-	+	-	+	-

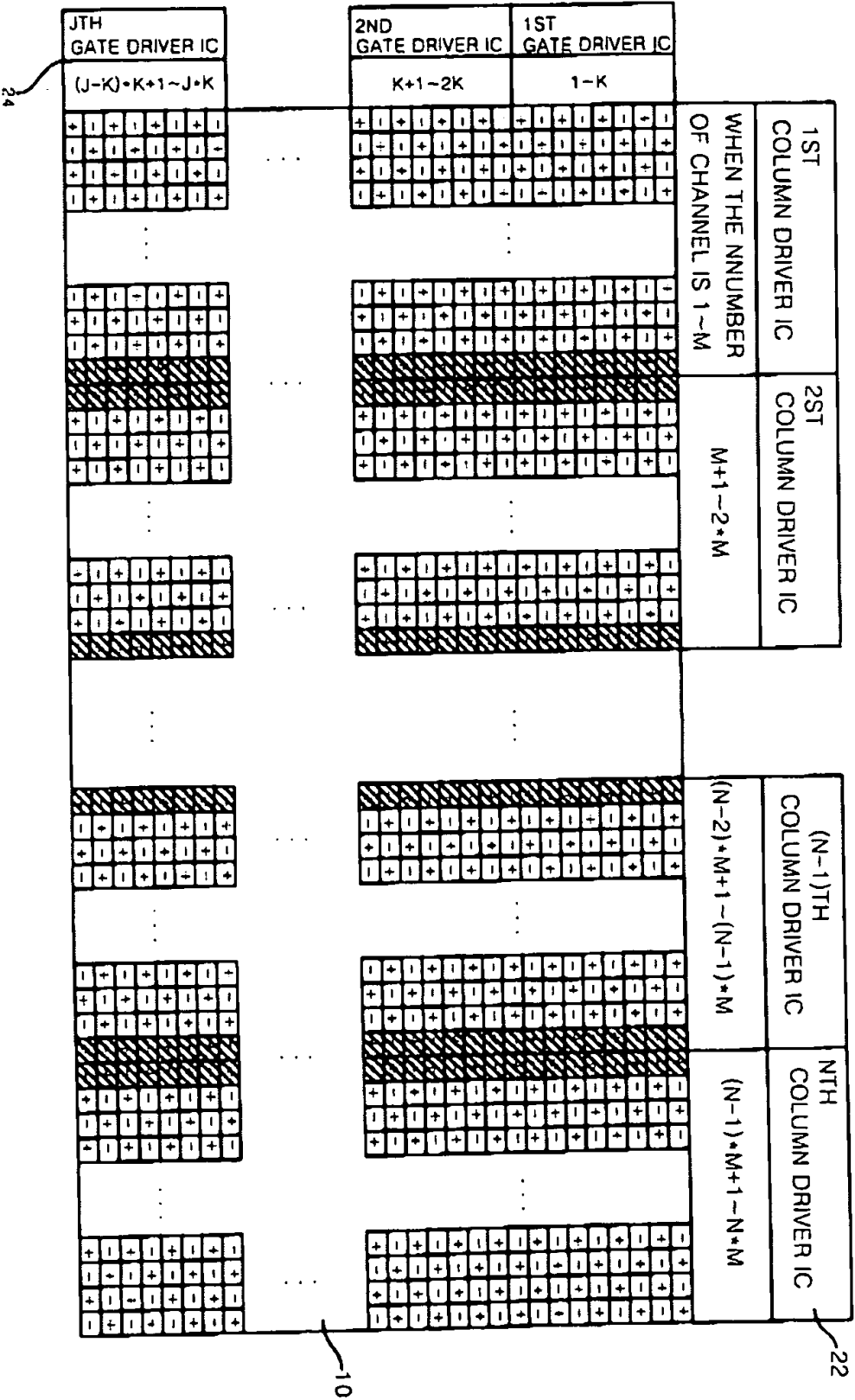
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FIG. 5A
PRIOR ART



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FIG. 5B
PRIOR ART



SECRET

FIG.6A

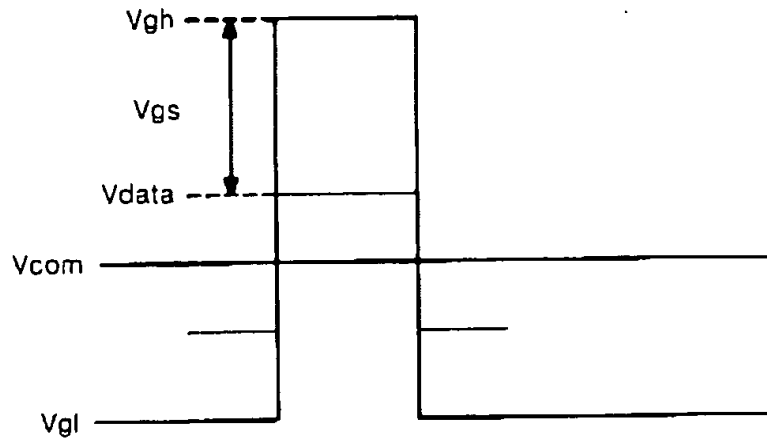
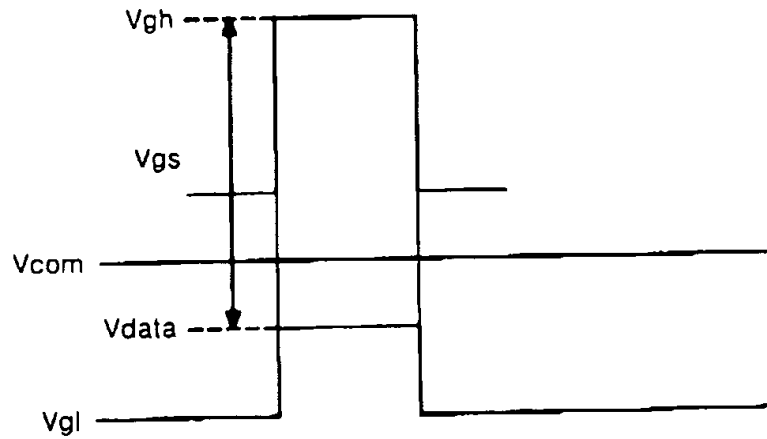
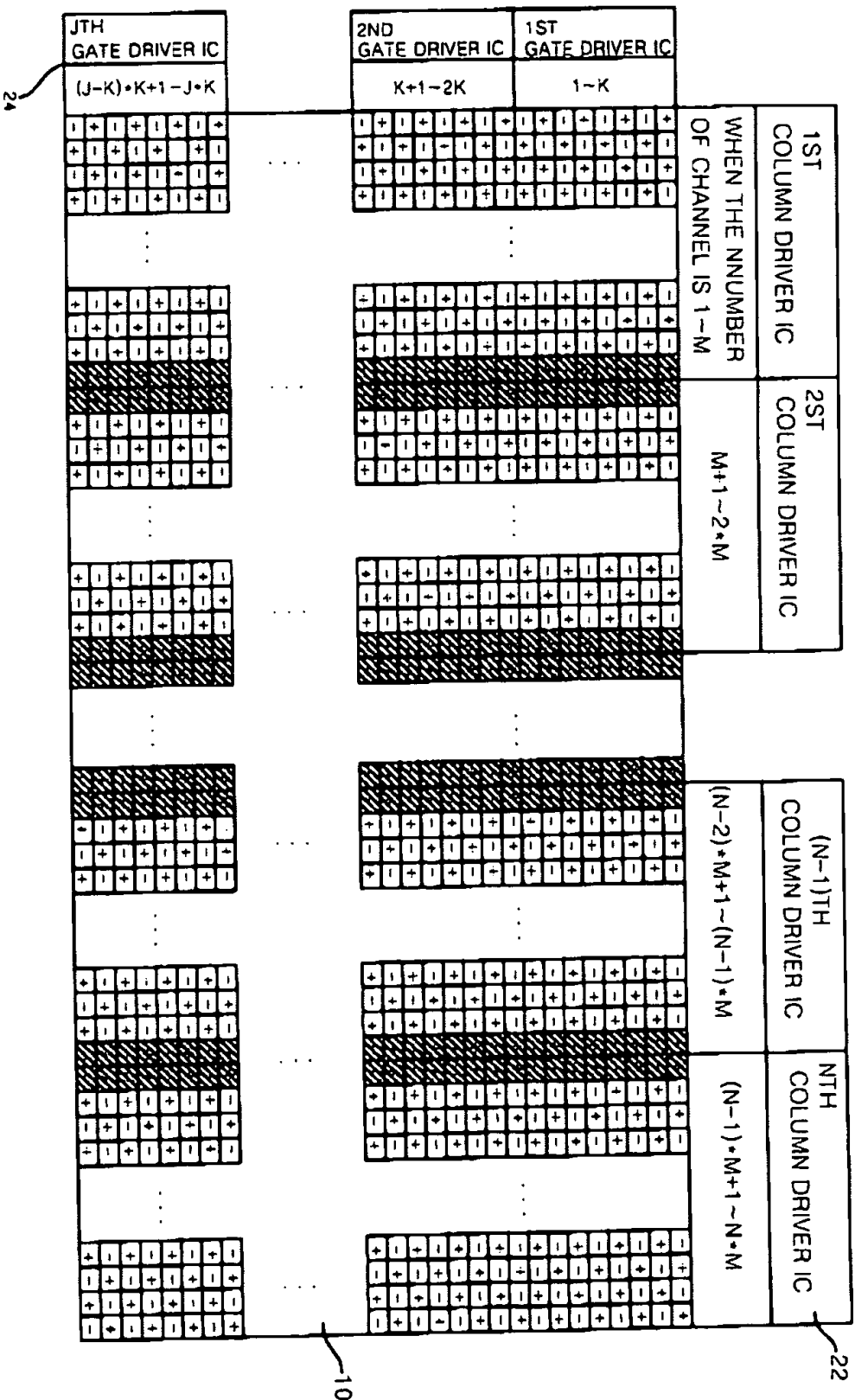


FIG.6B



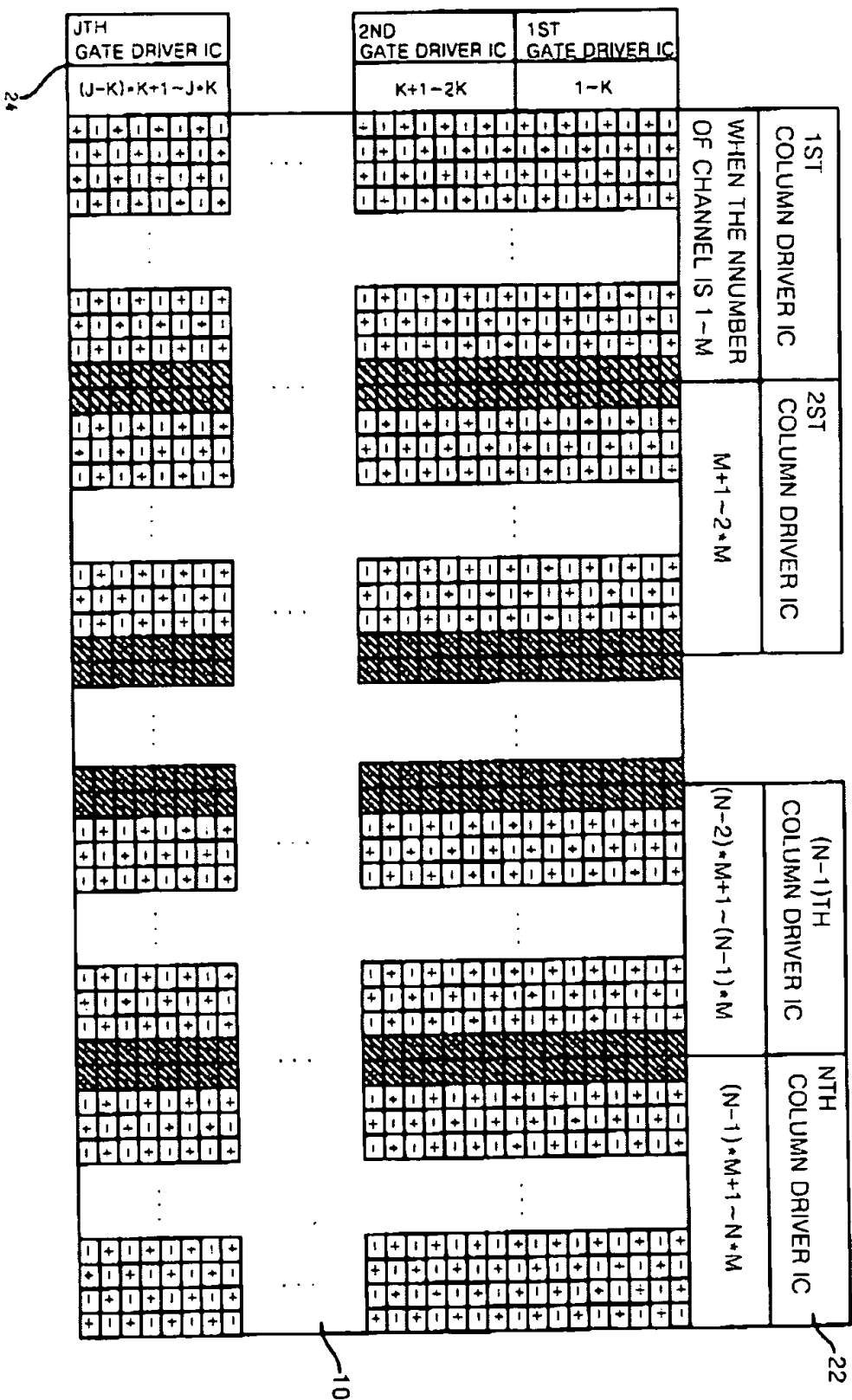
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FIG. 7A
PRIOR ART



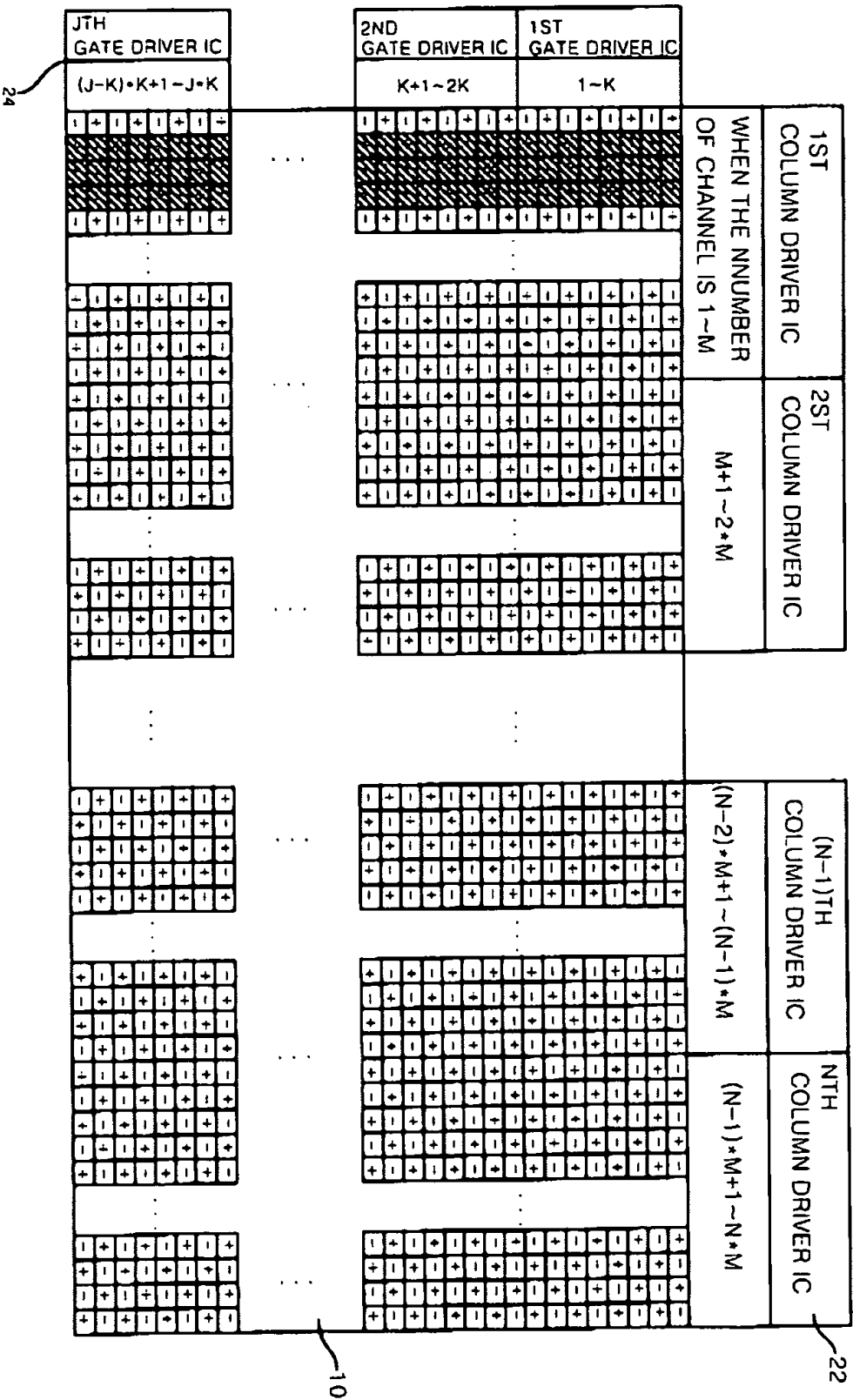
09054943.090100

FIG. 7B



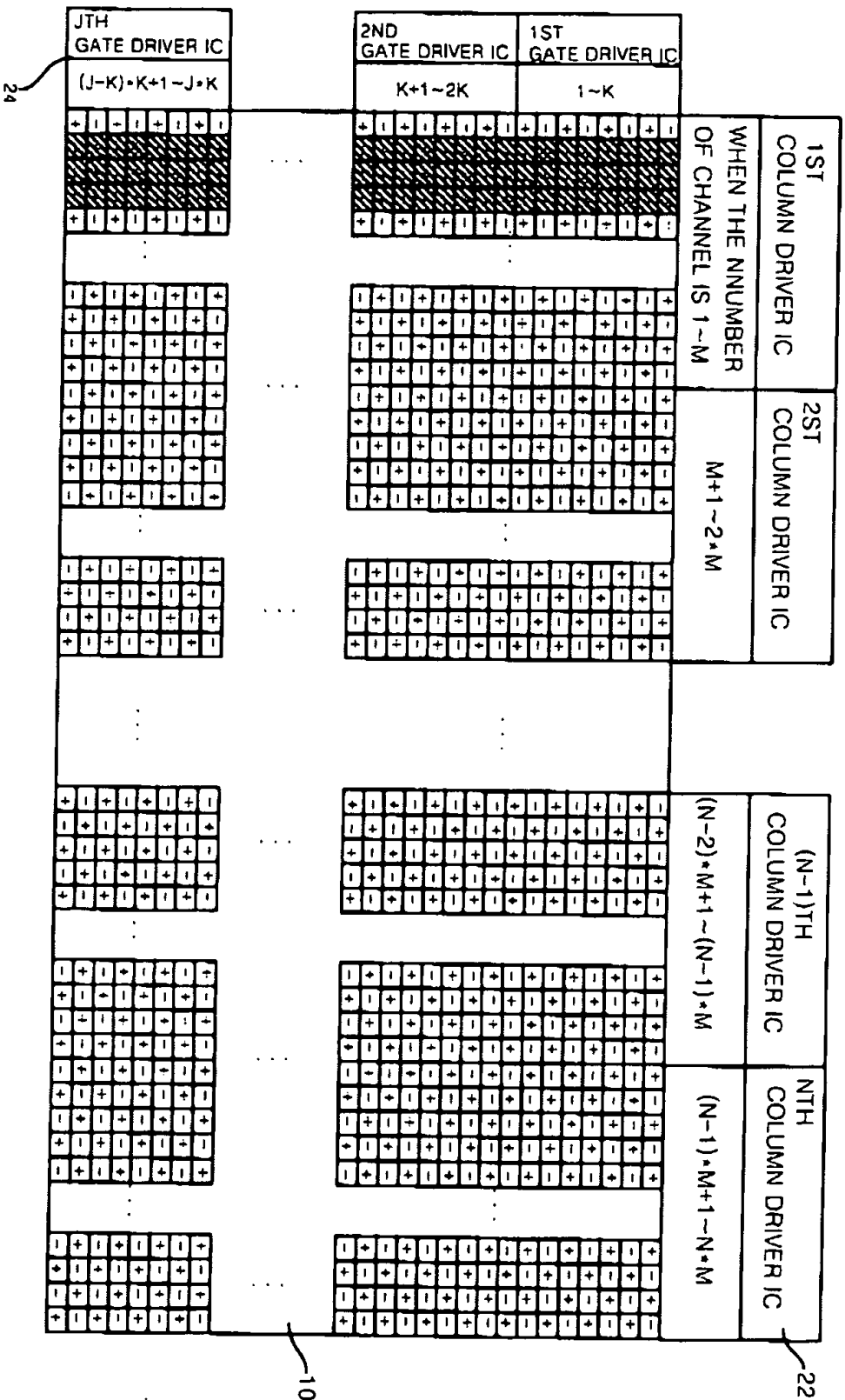
09654943 096106

FIG. 8A

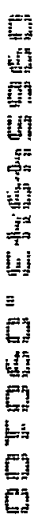


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FIG. 8B



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The timing diagram illustrates the relationship between the DENABLE signal and the output signals Vo1 and Vo2. The DENABLE signal is a clock signal with a period of 1H. The output signals Vo1 and Vo2 are shown as square waves. The LPOL signal is also shown as a square wave. The diagram includes timing parameters: DATA INTERVAL, 8ACLK, 16DCLK, and 8DCLK.

[illegible]